Remarks

The non-final Office Action dated July 29, 2008 lists the following rejections: claims 2, 4-5 and 10-19 stand rejected under 35 U.S.C. § 102(b) over Osawa *et al.* (U.S. Patent No. 5,946,247); claim 4 stands rejected under 35 U.S.C. 102(b) over Osawa *et al.* or under 35 U.S.C. § 103(a) in the alternative; claims 2, 4-5 and 10-19 stand rejected under 35 U.S.C. § 102(e) over Satoh (U.S. Patent No. 6,477,672); claims 2, 4-5 and 10-19 stand rejected under 35 U.S.C. § 103(a) over Abramovici *et al.* ("Digital Systems Testing and Testable Design" pgs. 479-487) and Osawa; claim 10 and intervening claims stand rejected under 35 U.S.C. § 101 and under 35 U.S.C. § 112(1-2). Applicant traverses all of the rejections and, unless explicitly stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action.

Applicant respectfully traverses the § 102(e) rejection of claims 2, 4-5 and 10-19 because the Office Action fails to assert correspondence between the Satoh reference and various aspects of the claimed invention, as discussed in response to the previous Office Action and as further discussed below. For example, the Satoh reference does not appear to teach programmable test vector generation as claimed. Applicant previously presented these arguments in the Response dated December 12, 2007, to which the Examiner failed to respond as required. *See, e.g.,* M.P.E.P. § 707.07(f) ("Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it."). In the instant Office Action, the Examiner simply repeats the rejection based upon the Satoh reference without responding in any manner to Applicant's previous arguments. Specifically, the Response to Arguments section of the instant Office Action only discusses the teaching of the Osawa reference, while failing to discuss the alleged correspondence between the Satoh reference and the claimed invention.

Moreover, the Office Action fails to assert correspondence between the Satoh reference and the various aspects of claims 2 and 11-19 as required. Specifically, the entire rejection of these claims consists of stating that "said claims do not depart in scope or spirit from the teachings of Satoh, and thus stand rejected on the same rationale as the rejection of claims 5 and 10." Applicant submits that claims 2 and 11-19 contain numerous aspects that are not disclosed by the cited portions of Satoh. As a first

example, the cited portions of Satoh do not teach that test head 300 (*i.e.*, the element that contains the memory under test MUT) includes a test response and analysis unit as claimed (*see, e.g.*, claims 2, 11 and 12-13). As a second example, the cited portions of Satoh do not teach programming the programmable test vector generator to provide pseudo-random test vectors and deterministic test vectors to the logic circuitry under test (*see, e.g.*, claims 15 and 19). As a third example, the cited portions of Satoh do not teach providing test vectors in real time to the logic circuitry under test (*see, e.g.*, claims 16 and 18).

In an effort to facilitate prosecution, Applicant has amended claim 10 to be directed to an arrangement that includes a tester and an integrated circuit having a test response analysis unit, and Applicant has amended claim 12 to include aspects of claim 13 directed to the integrated circuit including a test response analysis unit, as a result claim 13 has been cancelled. As discussed above, the cited portions of the Satoh reference do not teach or suggest such aspects directed to a test response analysis unit.

In view of the above, the cited portions of the Satoh reference do not correspond to numerous aspects of the claimed invention. Accordingly, the § 102(e) rejection of claims 2, 4-5 and 10-19 is improper and Applicant requests that it be withdrawn.

Applicant respectfully submits that the § 102(b) rejection of claims 2, 4-5 and 10-19 cannot stand because the cited portions of the Osawa reference do not correspond to the claimed invention which includes, for example, aspects directed to the integrated circuit, which includes the logic circuitry to be tested, also including a test response and analysis unit that receives test results form the logic circuitry and produces a compact representation of the results. Specifically, the cited portions of Osawa do not teach that tested circuit 31 (*i.e.*, semiconductor memory) includes a test response and analysis unit as claimed. The cited portions of Osawa also do not teach that RAM core 303 (*i.e.*, the memory being tested) includes a test response and analysis unit as claimed. *See, e.g.*, Figures 25 and 60 and the related discussion.

Regarding claims 5, 16 and 18, the cited portions of Osawa further do not correspond to aspects of the claimed invention directed to the programmable test vector generator being programmed to generate test vectors for the logic circuitry in real time. Regarding claim 17, the cited portions of Osawa further do not correspond to aspects of

the claimed invention directed to the programmable test vector generator being programmed to modify the test vectors based on the logic circuitry being tested. The portions of Osawa cited by the Office Action as allegedly corresponding to these aspects of the claimed invention (*i.e.,* Col. 89 line 5 *et seq.*) do not discuss generating test vectors in real time or modifying the test vectors based on the logic circuitry being tested.

In view of the above, the cited portions of the Osawa reference do not correspond to numerous aspects of the claimed invention. Accordingly, Applicant requests that the § 102(b) rejection of claims 2, 4-5 and 10-19 be withdrawn.

Applicant respectfully traverses the § 103(a) rejection of claims 2, 4-5 and 10-19 over Abramovici and Osawa. As admitted in the instant Office Action, Osawa does not teach programmable test generation. Abramovici relates to built-in self-testing of integrated circuits, and does not appear to disclose an external tester that includes a programmable test vector generator for testing logic circuitry. As such, any combination of Osawa and Abramovici, if proper, does not teach or suggest all the elements recited in Applicant's claims. Thus, a *prima facie* case of obviousness has not been stated. In addition, Applicant finds nothing in Abramovici, or any proposed combination of Osawa and Abramovici, to teach or suggest programming the programmable test vector generator to provide test vectors in real time to the logic circuitry under test, or to modify the test vectors based on the logic circuitry to be tested, as recited in claims 5 and 16-18.

Applicant previously presented these arguments to which the Examiner responded by asserting that each aspect of the claimed invention is disclosed by the Osawa reference. *See, e.g.,* section 3 of the Response to Arguments beginning on page 4 of the instant Office Action. As such, it is unclear to Applicant which aspects of Abramovici are being relied upon by the Examiner. Applicant respectfully requests clarification regarding what teachings of Abramovici the Examiner is proposing to combine with Osawa. Without such clarification, the Office Action fails to provide adequate detail regarding the proposed combination to enable Applicant to determine the propriety of such a combination. In order to comply with 35 U.S.C. § 132, sufficient detail must be provided by the Examiner regarding the alleged correspondence between the claimed invention and the cited reference to enable Applicant to adequately respond to the rejections. *See, also,* 37 CFR 1.104 ("The pertinence of each reference, if not apparent,

must be clearly explained and each rejected claim specified.") and M.P.E.P. § 706.02(j), ("It is important for an Examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply.")

In view of the above, the § 103(a) rejection of claims 2, 4-5 and 10-19 is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the § 101 rejection of claim 10 because the Office Action fails to present a proper basis for this rejection. The Office Action appears to assert that the tester of claim 10 does not include any circuitry; however, the tester of claim 10 does include circuitry such as a programmable test vector generator, which can include an arithmetic logic unit (claim 5), and a test response analysis unit (claim 4). Claim 10 is directed to a tester that generates test vectors. When the tester is connected to an IC that contains logic circuitry, the tester provides the test vectors to the logic circuitry and test results are provided back to the tester from the IC. *See, e.g.,* Applicant's Figures 3 and 4. As such, the claimed invention as a whole is useful. *See, e.g.,* M.P.E.P. § 2106(II)(A) ("The claimed invention as a whole must be useful and accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." **>*State Street Bank & Trust Co. v. Signature Financial Group Inc.*, 149 F.3d 1368, 1373-74, 47 USPQ2d 1596, 1601-02 (Fed. Cir. 1998).") Accordingly, the § 101 rejection of claim 10 is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the § 112(1) and § 112(2) rejections of claim 10 because claim 10 is fully supported/enabled by Applicant's disclosure and because the scope of claim 10 would be clear to the skilled artisan. As noted above, claim 10 is directed to a tester that generates test vectors. When the tester is connected to an IC containing logic circuitry, the tester provides the test vectors to the logic circuitry and test results are provided back to the tester from the IC. *See, e.g.,* Applicant's Figures 3 and 4. Thus, the generated test vectors are applied to the logic circuitry (*i.e.,* the "circuit under test"). As such, it would be clear to the skilled artisan that Applicant is claiming a tester (*e.g.,* element 2 of Applicant's Figure 3). Accordingly, the § 112(1) and § 112(2) rejections of claim 10 are improper and Applicant requests that they be withdrawn.

Moreover, Applicant submits that the amendments to claim 10 render the § 101, § 112(1) and § 112(2) rejections of claim 10 moot.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: _____
Name: Robert J. Crawford
Reg. No.: 32,122
651-686-6633
(NXPS.355PA)